

Amendments to the Claims

1-22. (Canceled).

23.(currently amended) A semiconductor memory device, comprising:
a silicon structure having a first conductivity type;
a gate electrode over the silicon structure;
a capacitor contact region in the silicon structure adjacent to one side of the gate electrode;
a bit line contact region in the silicon structure adjacent to the other side of the gate electrode;
a first dopant implant in the capacitor and bit line contact regions, the first dopant having a second conductivity type opposite the first conductivity type and the first dopant implant physically contacting the capacitor contact region; and
a second dopant implant in only the capacitor contact region.

24.(original) A device according to Claim 23, wherein the second dopant implant is deeper than the first dopant implant.

25.(original) A device according to Claim 24, wherein the depth of the first dopant implant is in the range of 500 angstroms to 1000 angstroms and the depth of the second dopant implant is up to 2,000 angstroms.

26.(previously presented) A semiconductor memory device, comprising:
a silicon structure having a first conductivity type;
a gate electrode over the silicon structure;
a capacitor contact region in the silicon structure adjacent to one side of the gate electrode;
a bit line contact region in the silicon structure adjacent to the other side of the gate electrode;
a first dopant implant in the capacitor and bit line contact regions, the first dopant having a second conductivity type opposite the first conductivity type;

insulating spacers extending along the sidewalls of the gate electrode and over a portion of the first dopant implant in the capacitor and bit line contact regions; and
a second dopant implant in only the capacitor contact region, the second dopant implant aligned with the insulating spacer extending over the capacitor contact region such that substantially all of the second dopant implant is formed in only that portion of the capacitor contact region not covered by the insulating spacer.

27.(previously presented) A semiconductor memory device, comprising:
a silicon structure having a first conductivity type;
a gate electrode over the silicon structure having a first conductivity type;
a capacitor contact region in the silicon structure adjacent to one side of the gate electrode;
a bit line contact region in the silicon structure adjacent to the other side of the gate electrode;
a first dopant implant in the capacitor and bit line contact regions, the first dopant having a second conductivity type opposite the first conductivity type;
insulating spacers extending along the sidewalls of the gate electrode and over a portion of the first dopant implant in the capacitor and bit line contact regions;
a second dopant implant in only the capacitor contact region, the second dopant implant aligned with the insulating spacer extending over the capacitor contact region such that substantially all of the second dopant implant is formed in only that portion of the capacitor contact region not covered by the insulating spacer;
a capacitor first conductor in electrical contact with the capacitor contact region;
a dielectric over the capacitor first conductor; and
a capacitor second conductor over the dielectric.

28.(currently amended) A semiconductor memory device, comprising:
a silicon structure having a first conductivity type;
a gate electrode over the silicon structure;
a capacitor contact region in the silicon structure adjacent to one side of the gate electrode;

a bit line contact region in the silicon structure adjacent to the other side of the gate electrode;

a first dopant implant in the capacitor and bit line contact regions, the first dopant having a second conductivity type opposite the first conductivity type, the first dopant implant physically contacting the capacitor contact region, and the first dopant implanted at a dosage of about 10^{13} ions per square centimeter at an implantation energy in the range of 20 KeV to 100 KeV;

insulating spacers extending along the sidewalls of the gate electrode and over a portion of the first dopant implant in the capacitor and bit line contact regions;

a second dopant implant in only the capacitor contact, the second dopant implant having the second conductivity type, and the second dopant implanted at a dosage of about 10^{13} ions per square centimeter at an implantation energy up to 200 KeV;

a capacitor first conductor in electrical contact with the capacitor contact region, the capacitor first conductor comprising polysilicon doped to the second conductivity type to a level in the range of 1×10^{19} to 1×10^{20} atoms per cubic centimeter;

a dielectric over the capacitor first conductor; and

a capacitor second conductor over the dielectric.

30.(previously presented) A semiconductor memory device, comprising:

a substrate;

a contact region in the substrate;

a first dopant implant in the contact region, the first implant defining a first implant profile; and

a second dopant implant in the contact region, the second implant defining a second implant profile narrower and deeper than the first implant profile.

31.(previously presented) A device according to Claim 30, wherein the first and second dopants have the same conductivity type.

32.(previously presented) A device according to Claim 31, further comprising a capacitor in electrical contact with the contact region.

33.(previously presented) A device according to Claim 32, wherein the depth of the first dopant implant is in the range of 500 angstroms to 1000 angstroms and the depth of the second dopant implant is up to 2,000 angstroms.

34.(new) A device according to Claim 26, wherein the second dopant implant is narrower and deeper than the first dopant implant.

35.(new) A device according to Claim 34, wherein the depth of the first dopant implant is in the range of 500 angstroms to 1000 angstroms and the depth of the second dopant implant is up to 2,000 angstroms.

36.(new) A device according to Claim 27, wherein the second dopant implant is narrower and deeper than the first dopant implant.

37.(new) A device according to Claim 36, wherein the depth of the first dopant implant is in the range of 500 angstroms to 1000 angstroms and the depth of the second dopant implant is up to 2,000 angstroms.

Respectfully submitted,



Steven R. Ormiston
Attorney for Applicants
Registration No. 35,974
(208) 433-1991

CERTIFICATE OF FACSIMILE

I hereby certify that this correspondence is being facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below to facsimile number (703) 872-9306.

Date of Deposit: December 10, 2003

Typed or printed name: Tanra F. Paulin

Signature: 